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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/674,317	09/29/2003	Ying-Ren Lin	59970 (71987)	4629

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EXAMINER	
CARPIO, IVAN HERNAN	

ART UNIT	PAPER NUMBER
2841	

DATE MAILED: 04/26/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

HA

Office Action Summary	Application No.	Applicant(s)	
	10/674,317	LIN ET AL.	
	Examiner	Art Unit	
	Ivan H. Carpio	2841	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *23 January 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-7 and 9-15* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-7 and 9-15* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *29 September 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

Applicant's arguments with respect to claims 1-15 have been considered but are moot in view of the new ground(s) of rejection.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-6 and 9-15 are rejected under 35 U.S.C. 103(a) as being unpatentable over applicant's admitted prior art (aapa from here on) in view of Tay (US 2004/0113285).

With respect to claim 1 the aapa teaches a semiconductor package having a substrate comprising a dielectric layer (Fig. 5A, element 100) and a solder mask layer (Fig. 5A, element 102) on the dielectric layer, the solder mask layer having a plurality of openings (Fig. 5A, element 102b), the ground pad structure, comprising: a ground plane (Fig. 5A, element 108), which is made of a conductive material and provided on the dielectric layer and covered by the solder mask layer (Fig. 5a, element 102a) of the substrate; and a plurality of ground pads (Fig. 5a, element 108 at the openings 102a) formed on the ground plane and exposed from the opening of the solder mask layer.

The aapa does not teach that a part of the ground pads, which are located on the circumference of the ground plane are non-solder mask defined ground pads, such that a portion of the dielectric layer surrounding the non-solder mask defined ground pads is exposed form the solder mask layer. Tay teaches a part of the ground pads (Fig. 5c, element 32), which are located on the circumference of the ground plane are non-solder mask defined ground pads, such that a portion of the dielectric layer (Fig. 5c, element 56) surrounding the non-solder mask defined ground pads is exposed form the solder mask layer. It would have been obvious to one of ordinary skill in the art at the time of the invention to use the non-solder mask defined pad structure, taught by Tay, with the semiconductor package, taught by the applicant's admitted prior art, for the purpose of reducing cracking of the electrical interconnection and resist the crack propagation (Tay paragraph [0025]).

With respect to claim 2 and with all the limitations of claim 1, Tay teaches that the non-solder mask defined ground pads disposed on the circumference of the ground plane are protruded from and partially extended (Fig. 5A) from the circumference of the ground plane.

With respect to claim 3 and with all the limitations of claim 2, the aapa teaches wherein the ground pads are arranged in a matrix array (Fig.5B).

With respect to claim 4 and with all the limitations of claim 2, the aapa teaches that the ground plane is disposed on a central portion (Fig. 5A) of the substrate of the semiconductor package.

With respect to claim 5 the aapa teaches a substrate (Fig. 5a, element 10), which has a dielectric layer (Fig. 5A, element 100), a plurality of conductive traces (Fig. 5A, element 101, 104) disposed above and beneath the dielectric layer, and a solder mask layer (Fig. 5A, element 102) for covering the conductive traces and the dielectric layer and having a plurality of openings (Fig. 5A, 102a,b), wherein a non-ground pad (Fig. 5A, element 10-3) is formed on a terminal of each of the conductive traces and exposed from one of the openings; a ground pad structure, which has a ground plane (Fig. 5A, element 108) made of a conductive material, and a plurality of ground pads (Fig. 5a, element 108 at the openings 102a) formed on the ground plane, wherein the ground plane is provided on the dielectric layer of the substrate and covered by the solder mask, and the ground pads are exposed from the openings of the solder mask, a semiconductor chip (Fig. 5a, element 11), which has an active surface and a corresponding inactive surface, the active surface being formed with a plurality of non-ground conductive metal solder means and ground conductive metal solder means so as to electrically solder the non-ground conductive metal solder means and ground conductive metal solder means of the semiconductor chip to the corresponding non-ground pads and ground pads on the substrate; an encapsulant body (Fig. 5a, element 12), which encapsulates the semiconductor chip, the conductive metal solder means, the solder mask layer, and the portion of the dielectric layer surrounding the non-solder mask defined ground pads; and a plurality of conductive elements under the substrate. The aapa does not teach that a part of the ground pads, which are located on the circumference of the ground plane are non-solder mask defined ground pads, such that

a portion of the dielectric layer surrounding the non-solder mask defined ground pads is exposed form the solder mask layer. Tay teaches a part of the ground pads (Fig. 5c, element 32), which are located on the circumference of the ground plane are non-solder mask defined ground pads, such that a portion of the dielectric layer (Fig. 5c, element 56) surrounding the non-solder mask defined ground pads is exposed form the solder mask layer. It would have been obvious to one of ordinary skill in the art at the time of the invention to use the non-solder mask defined pad structure, taught by Tay, with the semiconductor package, taught by the applicant's admitted prior art, for the purpose of reducing cracking of the electrical interconnection and resist the crack propagation (Tay paragraph [0025]).

With respect to claim 6 and with all the limitations of claim 5, the aapa teaches that the semiconductor package is a flip-chip semiconductor package.

With respect to claim 9 and with all the limitations of claim 5, Tay teaches that the non-solder mask defined ground pads disposed on the circumference (Fig. 5A) of the ground plane are protruded from and partially extended from the circumference of the ground plane.

With respect to claim 10 and with all limitations of claim 5, the aapa teaches that the non-ground pads are non-solder mask defined (Fig. 5A, 103) non-ground pads.

With respect to claim 11 and with all the limitations of claim 10, the aapa teaches that the non-solder mask defined non-grounds are exposed from openings of the insulative layer, each opening being sized larger (Fig. 5A, element 102b)than the corresponding non-ground pad for exposing the non-ground pad.

With respect to claim 12 and 13 with all the limitations of claim 5, the aapa teaches that the conductive metal solder means are solder balls (Fig. 5A, element 112).

With respect to claim 14 and with all the limitations of claim 5, the aapa teaches that the non-ground pads and the ground pads are arranged in a matrix array (Fig. 5B).

With respect to claim 15 and with all the limitations of claim 5, the aapa teaches that the ground plane is disposed on a central portion (Fig. 5A) of the substrate.

Claim 7 is rejected under 35 U.S.C. 103(a) as being unpatentable over the aapa in view of Jones (US Patent 5541450).

With respect to claim 7 and with all the limitations in claim 1, the aapa teaches all of the limitations but does teach specifically that the dielectric layer is made of an insulative material selected from the group consisting of Bismaleimide Triazine Resin, Polyimide, FR-4 Resin and FR-5 Resin. Jones teaches a dielectric layer made of Bismaleimide Triazine Resin or FR-4 Resin (column 2, lines 17-19). It would have been obvious to make the dielectric layer taught by the aapa because since in semiconductor applications it is typically (column 2, lines 17-19) made from Bismaleimide Triazine Resin or FR-4 Resin, manufacturing parts and process would be easy to find and cost effective.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ivan H. Carpio whose telephone number is 571-272-8396. The examiner can normally be reached on M-R 6:00am - 4:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kammie Cuneo can be reached on 571-272-1957. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

IC

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SPE 2841